RISC-V & Open Source
Fundaments for European Processor Sovereignty

EuroHPC Summit

The European Chips Act and the development of European processors for HPC

22 March 2022

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NXP Semiconductors

Recommendations and Roadmap for European Sovereignty in Open Source Hardware, Software, and RISC-V Technologies

Report from the

Open Source Hardware & Software Working Group

November 2021

Members of the Open Source HW/SW Working Group

- *Chair :*
  - Patrick Pype — NXP Semiconductors
- *Participants :*
- Jan Andersson — Cobham Gaisler
- Luca Benini — ETH Zürich / Univ. Bologna
- Sven Beyer — Siemens
- Holger Blasum — SYSGO GmbH
- Sylvain Depierre — NanoXplore
- Marc Duranton — CEA
- Wolfgang Ecker — Infineon
- Michael Gielda — Antmicro Ltd
- Edwin Hakkennes — Technolution
- Andreas Koch — Technische Universität Darmstadt
- Loic Lietar — GreenWaves Technologies
- Andreas Mauderer — Bosch
- Jan-Hendrik Oetjens — Bosch
- Jérôme Quévremont — Thales
- John Round — NXP Semiconductors
- Javier Serrano — CERN
- Herbert Taucher — Siemens

What is RISC-V ?

- Open standard instruction set architecture
- Provided under open-source licenses with no fees to use
- Initially designed for academic use and educational purposes
- Is the starting point for designing a HW processor in a certain process technology
- “RISC-V International’’ owns, maintains and publishes IP related to RISC-V – only specification, no implementation

RISC-V IP to SoC landscape

Base Building Blocks

High-end RISC-V core

Mid-end RISC-V core

Low-end RISC-V core

Other SoC IPs
(interconnect, peripherals…)

RISC-V is a modular ISA:
- Basic
- Standard extensions
- Custom extensions

Software
(OS, tool chains, compilers, drivers, debuggers…)

Domain-specific features
(safety, security, acceleration, AI…)

Custom RISC-V extensions

Co-processors / accelerators

Customized solutions for various markets

Automotive

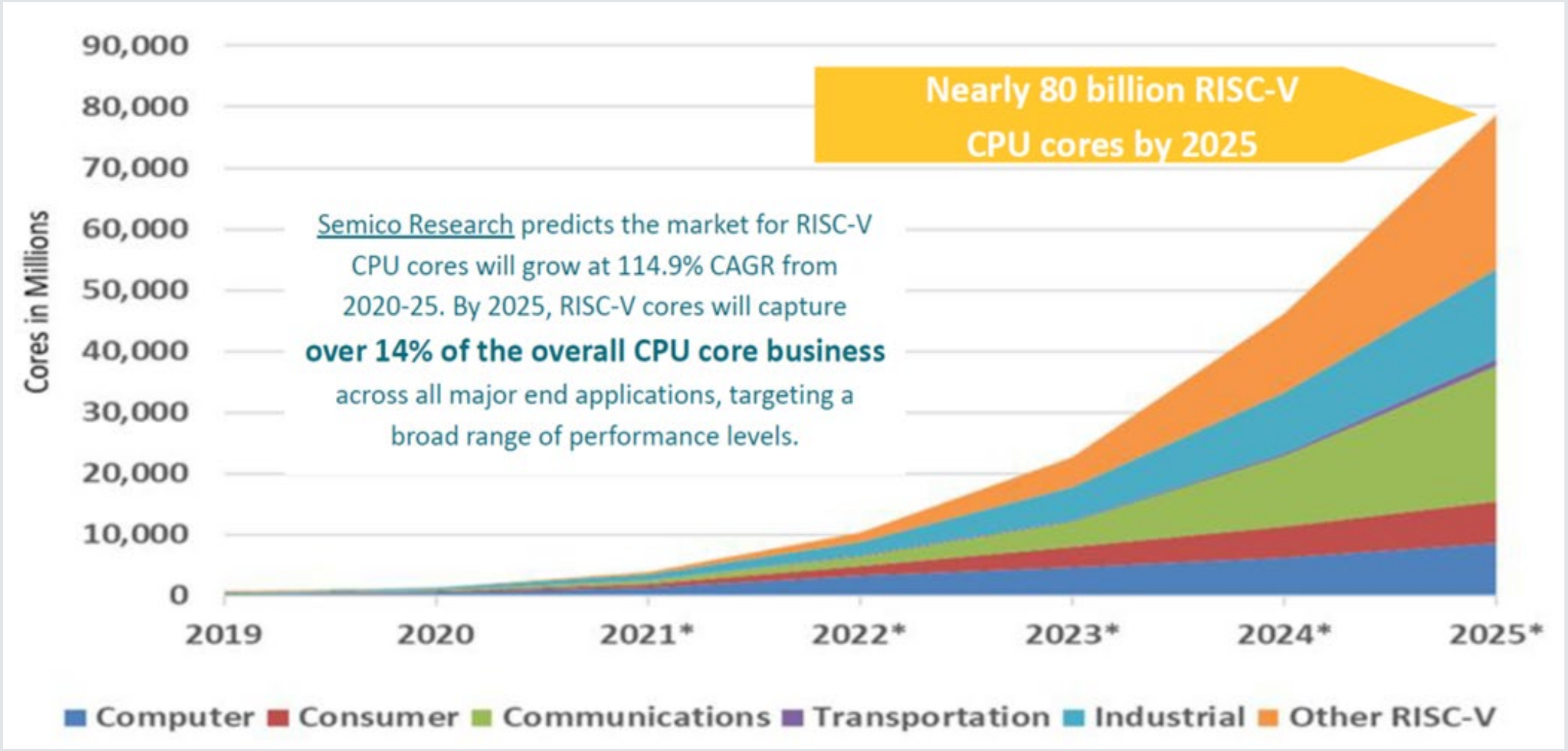
Industrial

Communication

HPC

Other sectors

RISC-V Usage



Source: Semico Research Corp., March 2021

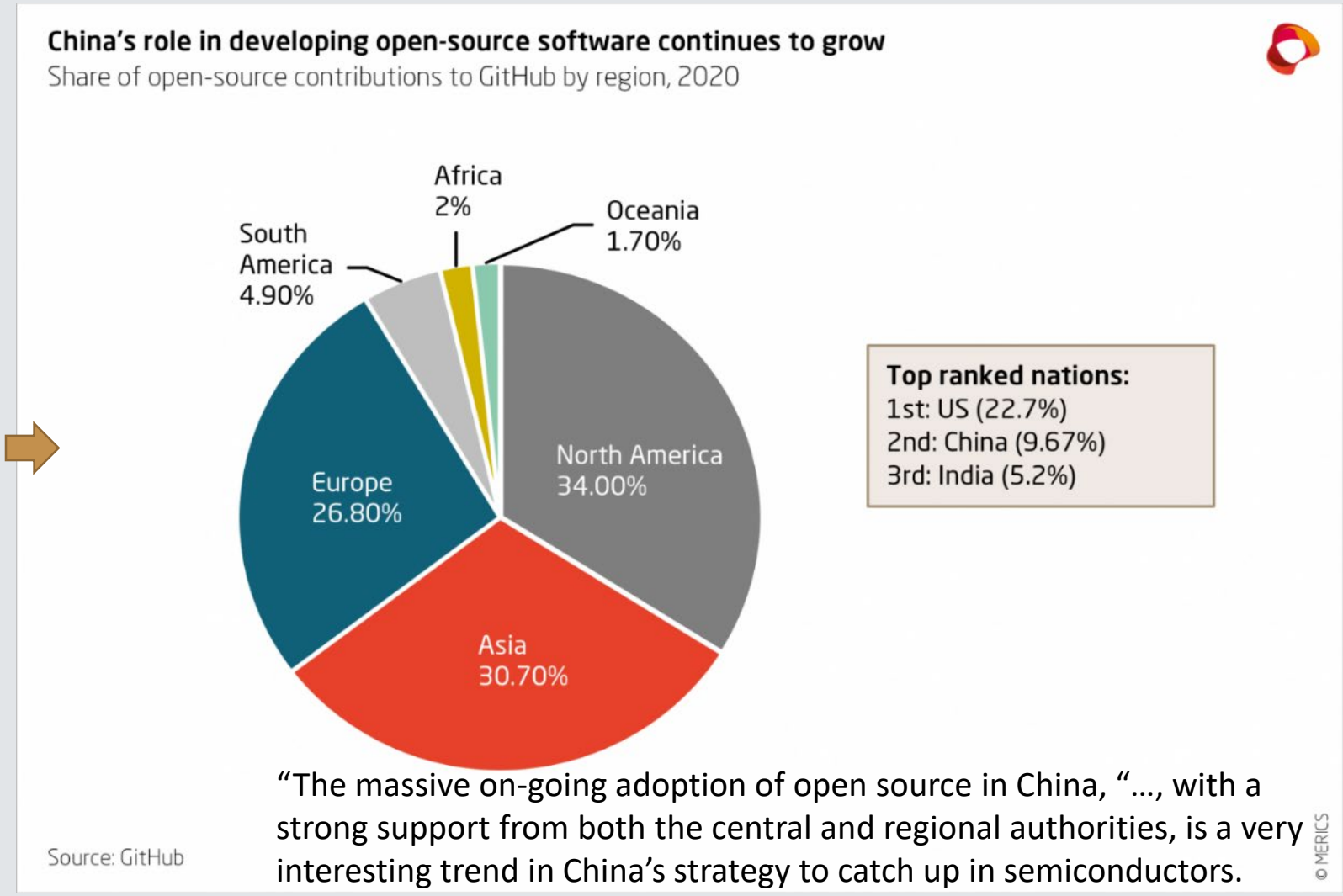
"23% of projects in both the ASIC and FPGA spaces incorporated at least one RISC-V processor."

(Source: Wilson Research Group Functional Verification, 2020)

Open Source in China

HW → "Alibaba introduced first RISC-V based product (XT910) in July 2020"
(Source : https://www.nextplatform.com/2020/08/21/alibaba-on-the-bleeding-edge-of-risc-v-with-xt910/)

SW →



"The massive on-going adoption of open source in China, "…, with a strong support from both the central and regional authorities, is a very interesting trend in China's strategy to catch up in semiconductors.

"For China, open source is an **industrial policy tool** and important part of its **push for technological autonomy**"

Source : https://merics.org/en/short-analysis/china-bets-open-source-technologies-boost-domestic-innovation

Why RISC-V in Europe ?

STRENGTHS
- Easy access & low barrier for SoC design
- Ability to customize
- Accessible data for safety & security analysis (whitebox)
- Availability of SW ecosystem
- Lower export control restrictions
- Less vulnerable to geo-political risks
- Strong academic support ; educational use
- Steers Innovation

WEAKNESSES
- Not Industrial Quality IP yet (HW/SW)
- Long-term guaranteed support to industrial users not yet established
- Risk of maintenance
- Lack of some IP (e.g. interconnect)

OPPORTUNITIES
- Customization opportunities
- Sharing development costs
- Sharing support costs
- New licensing models
- Support to SME's
- New industrial leaders

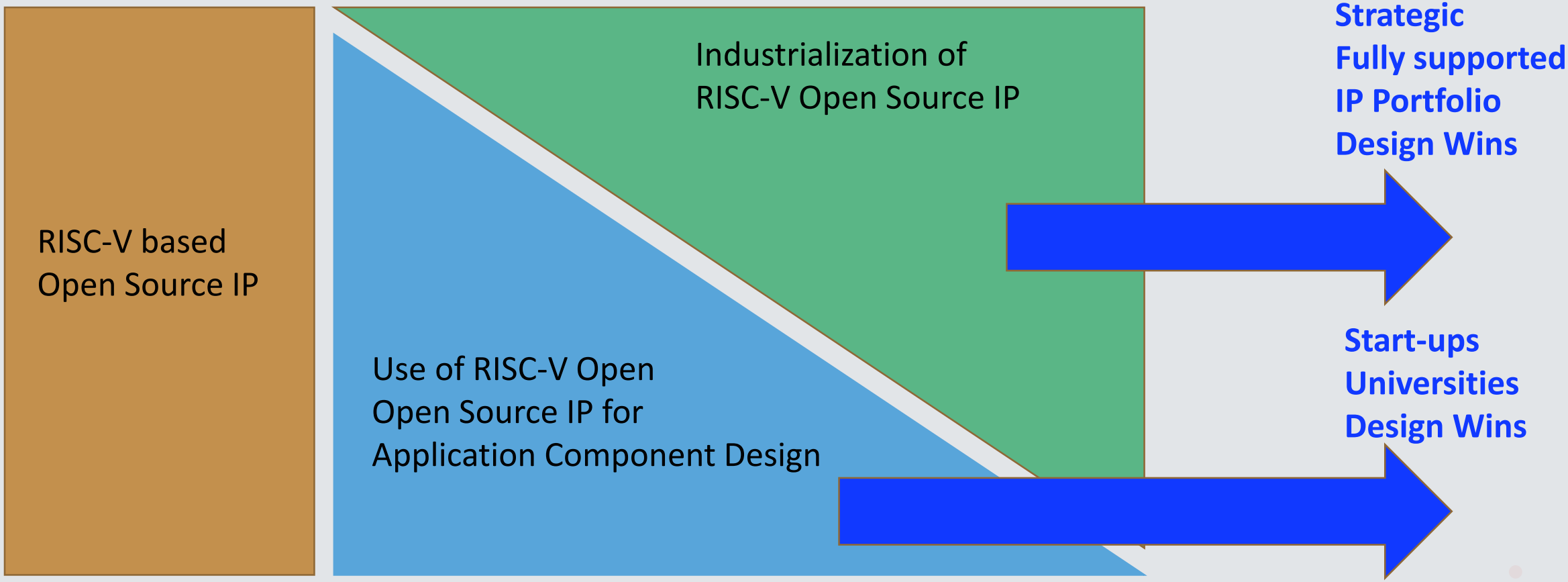
MAXIMISE

THREATS
- Risk not to create enough critical mass in Europe
- US/China competitors are running fast, with large investments and acceptance by leading end-user companies

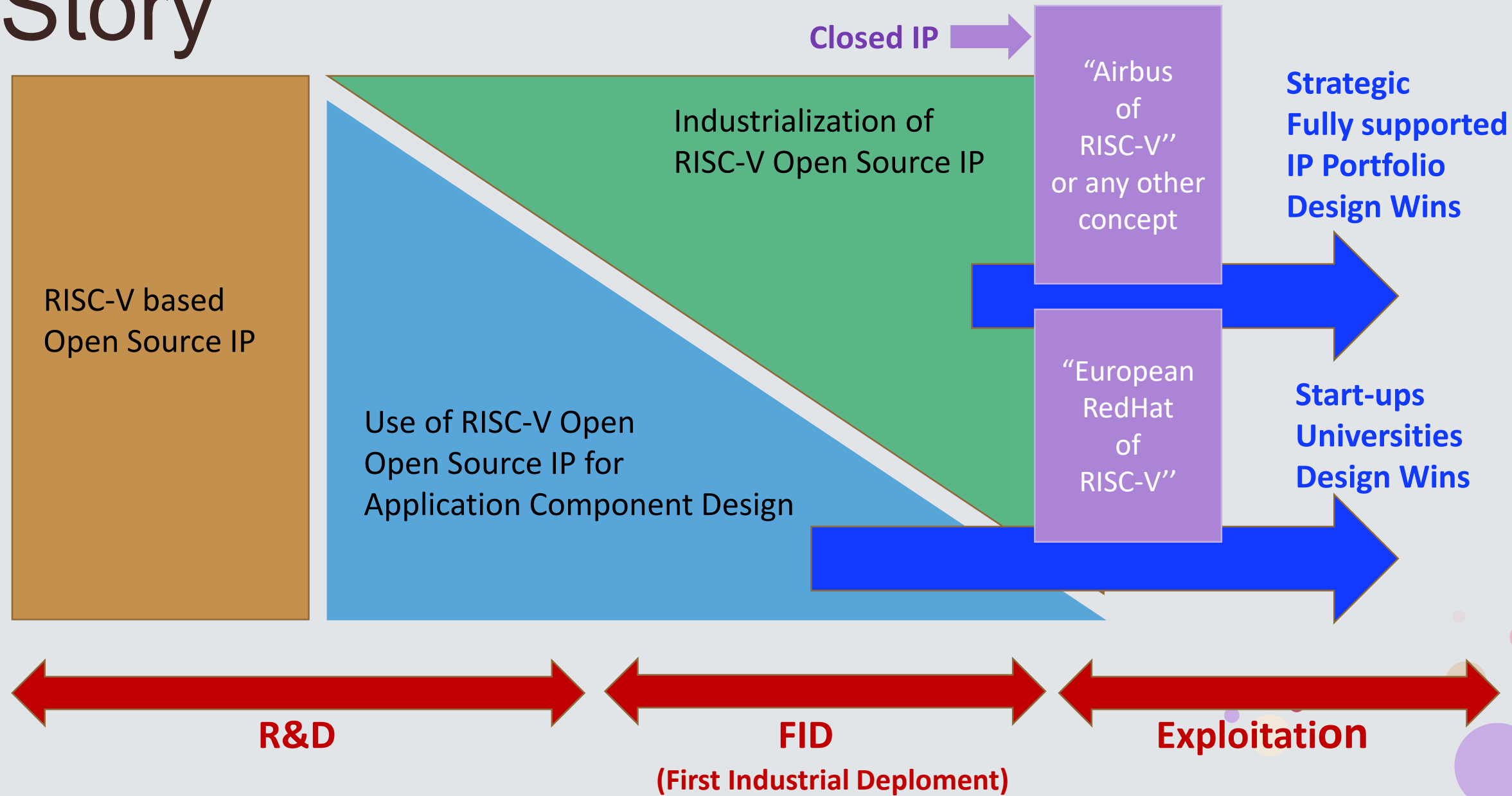
RESOLVE

Europe must develop the RISC-V supply chain to support autonomy in critical market sectors and reduce its dependency on US & China

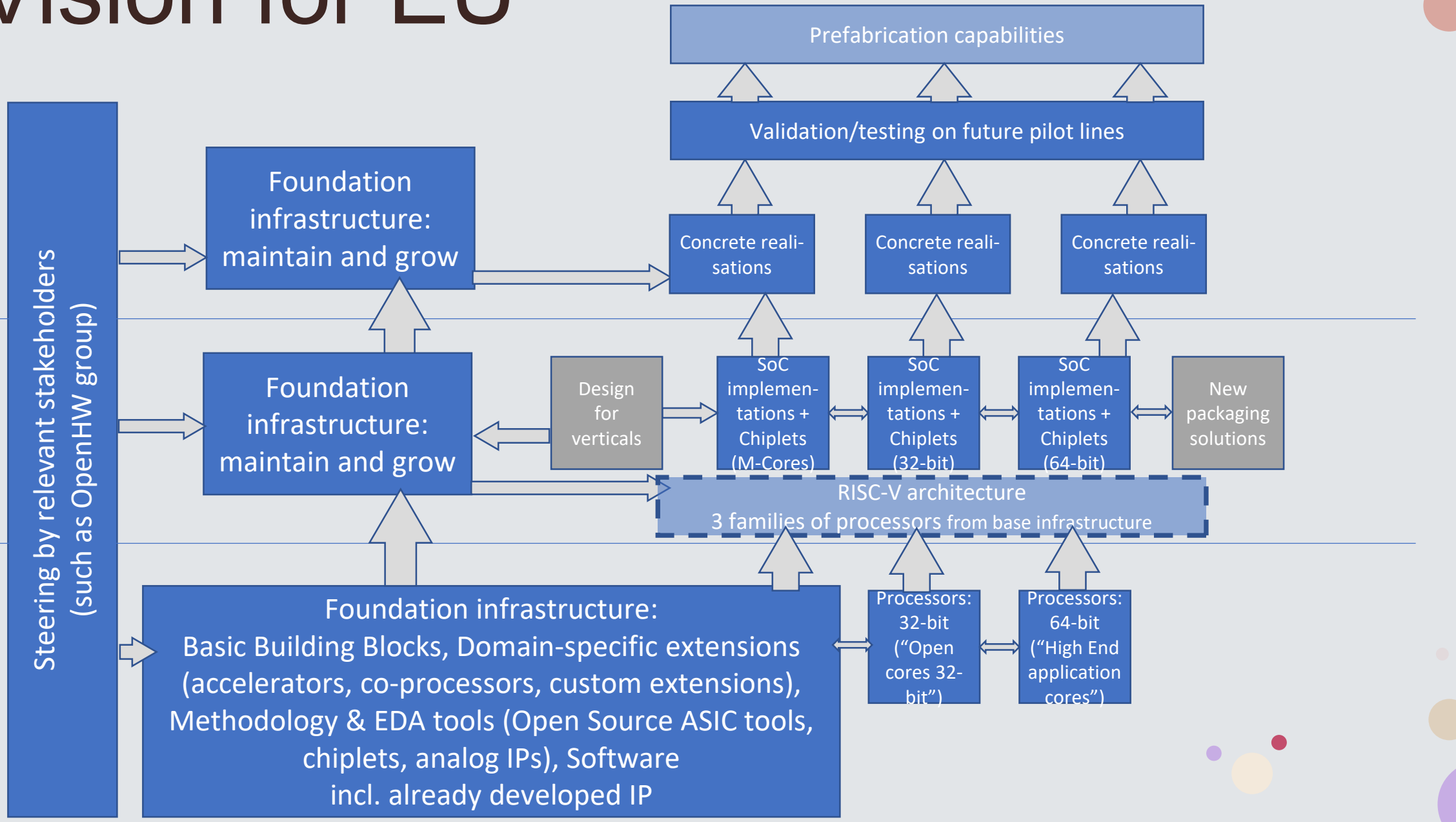
Approach to European Success Story



Approach to European Success Story



Vision for EU



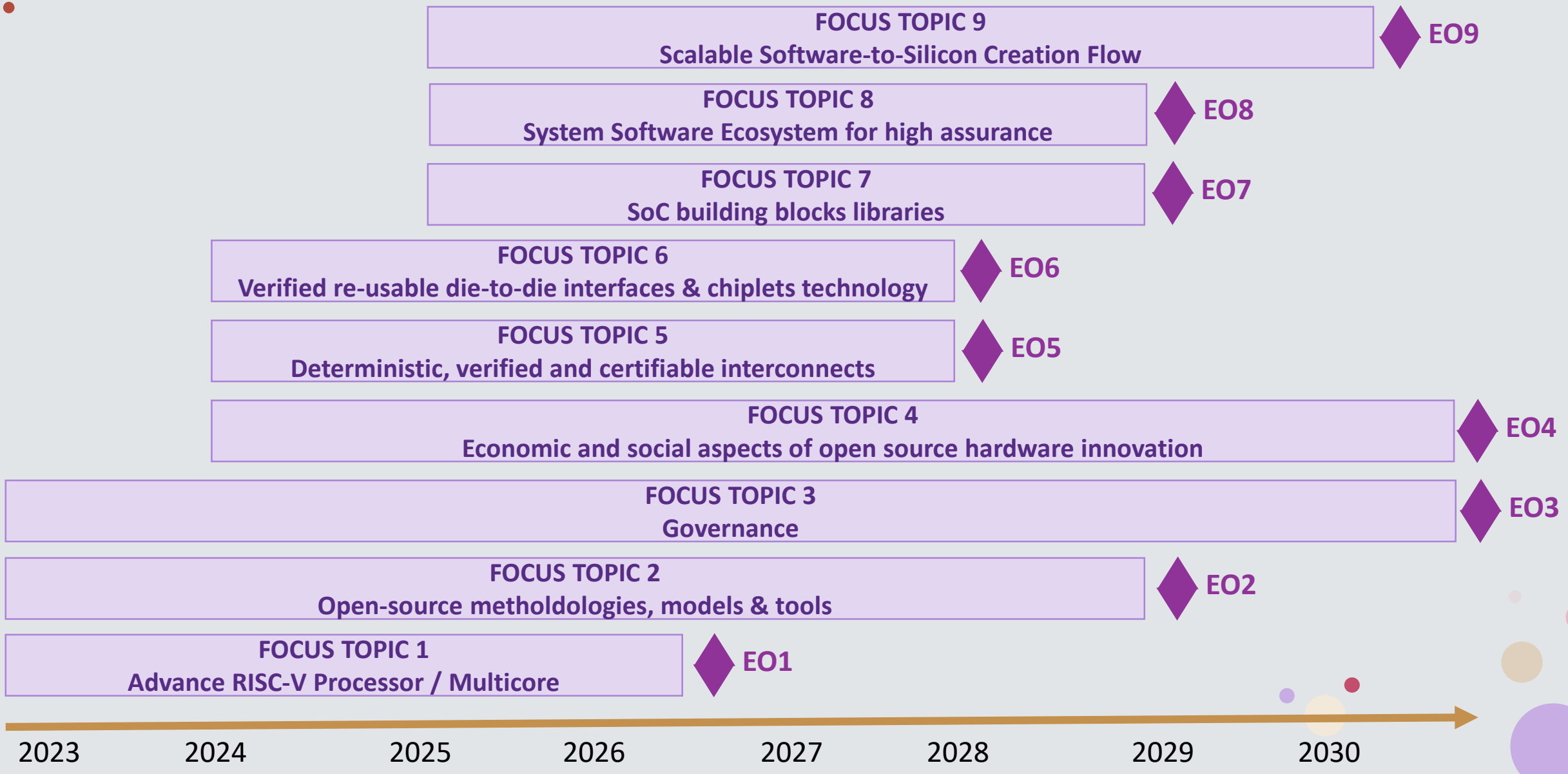
How to realize the vision ?

- Part of Phase 2 of the Working Group – draft report available March 7th, 2022
- This report contains the following items :
  - Value of RISC-V and Open Source IP and how to create business on the market, including business strategies, business models and licensing approaches
  - Gaps and future needs for RISC-V and OpenSource IP
  - Roadmap of Implementation Programs by means of Focus Topics

VISION → **ROADMAPS** → **FOCUS TOPICS IMPLEMENTATION PLAN**

Short term (2-5 years)
Mid term (5-10 years)
Long Term (> 10 years)

Planning of Focus Topics & Expected Outcomes



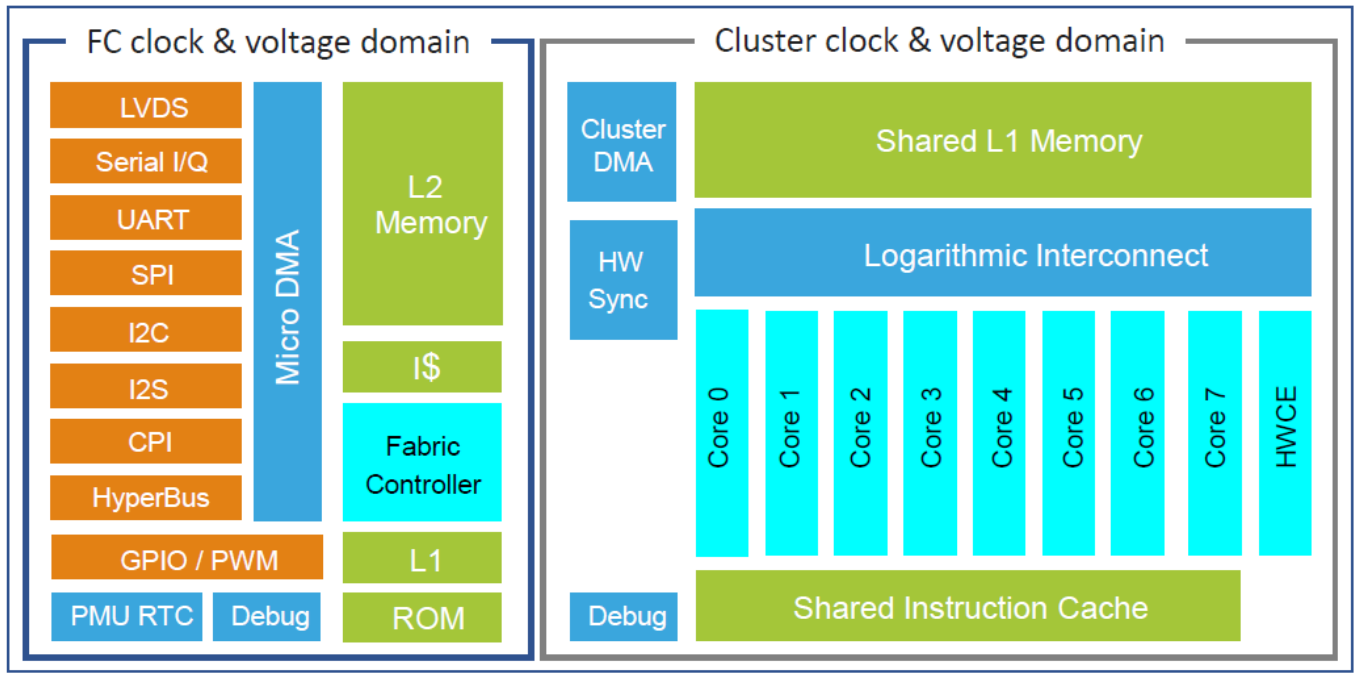
Conclusions & Next Steps

- Europe needs to act **FAST**
  - **F** **F**irmly
  - **A** **A**ct
  - **S** **S**trongly
  - **T** **T**oday

- Next steps:
  - Ensure enough RDI investments by all involved stakeholders ~ 1 Billion € program over 10 years
  - Active involvement with and commitment from end-user companies
  - Need for industrial leadership to get a professional European long term supported and maintained RISC-V based processor organization

Let's build further upon EU Success Stories, e.g. GAP8 IoT processor

Two independent clock and voltage domains, from 0-133MHz/1V up to 0-250MHz/1.2V



MCU Function
- Extended RISC-V core
- Extensive I/O set
- Micro DMA
- Embedded DC/DC c
- Secured execution

Computation engine
- 8 extended RISC
- Fully programmable
- Efficient parallelization
- Shared instruction cache
- Multi channel DMA
- HW synchronization
- HW convolution Engine

PULP
Parallel Ultra Low Power

Zero-Riscy RISCV core
Interco, DMAs, peripherals

GREENWAVES TECHNOLOGIES

greenwaves-technologies.com