SIPEARL

Sovereignty in motion

EuroHPC Summit Week, March 2022

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Chief Strategy Officer

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Company Update

SIPEARL CORPORATE OVERVIEW

The European Server Processor Solution

- HQ: Maisons-Laffitte (Paris area), France
- Incorporated in June 2019
- CEO and Founder, Philippe Notton
- Key Personnel from Intel, Infineon, Atos, ST, Marvell, Nokia, MStar-Mediatek
- HPC targeted processor based on Arm Neoverse V1 cores
- **Targeting >1000 employees <2026**

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R&D OFFICES & PARTNER/CUSTOMER PROXIMITY

Reims
SiPearl DataCenter #1

Eppe
SiPearl DataCenter #2

Maisons Laffitte
Head-Quarters

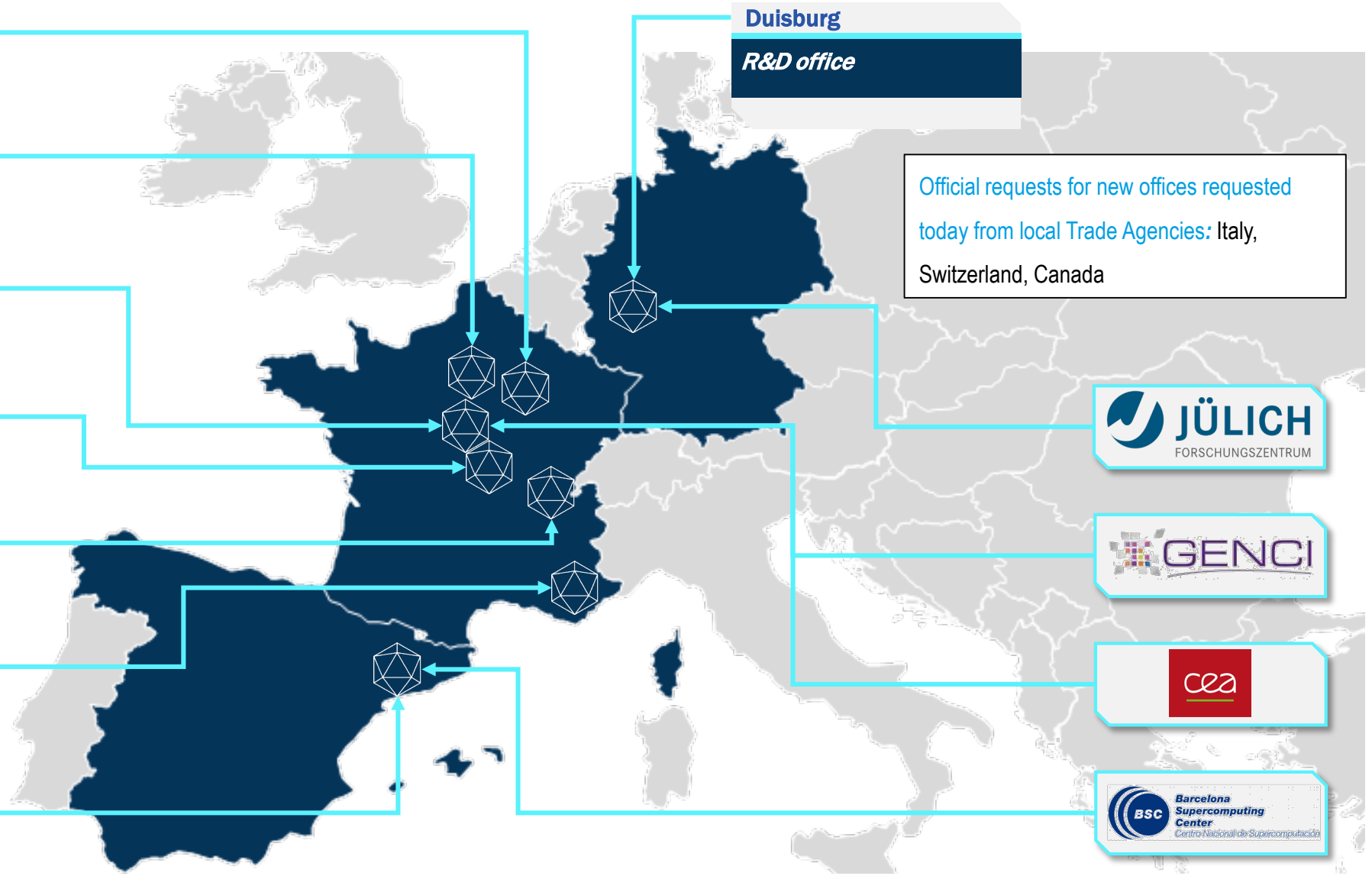
Maisons-Laffitte
R&D office

Grenoble
R&D office

Sophia-Antipolis
R&D office

Barcelona
R&D office

Duisburg
R&D office



Official requests for new offices requested today from local Trade Agencies: Italy, Switzerland, Canada

JÜLICH FORSCHUNGSZENTRUM

GENCI

cea

BSC Barcelona Supercomputing Center Centro Nacional de Supercomputación

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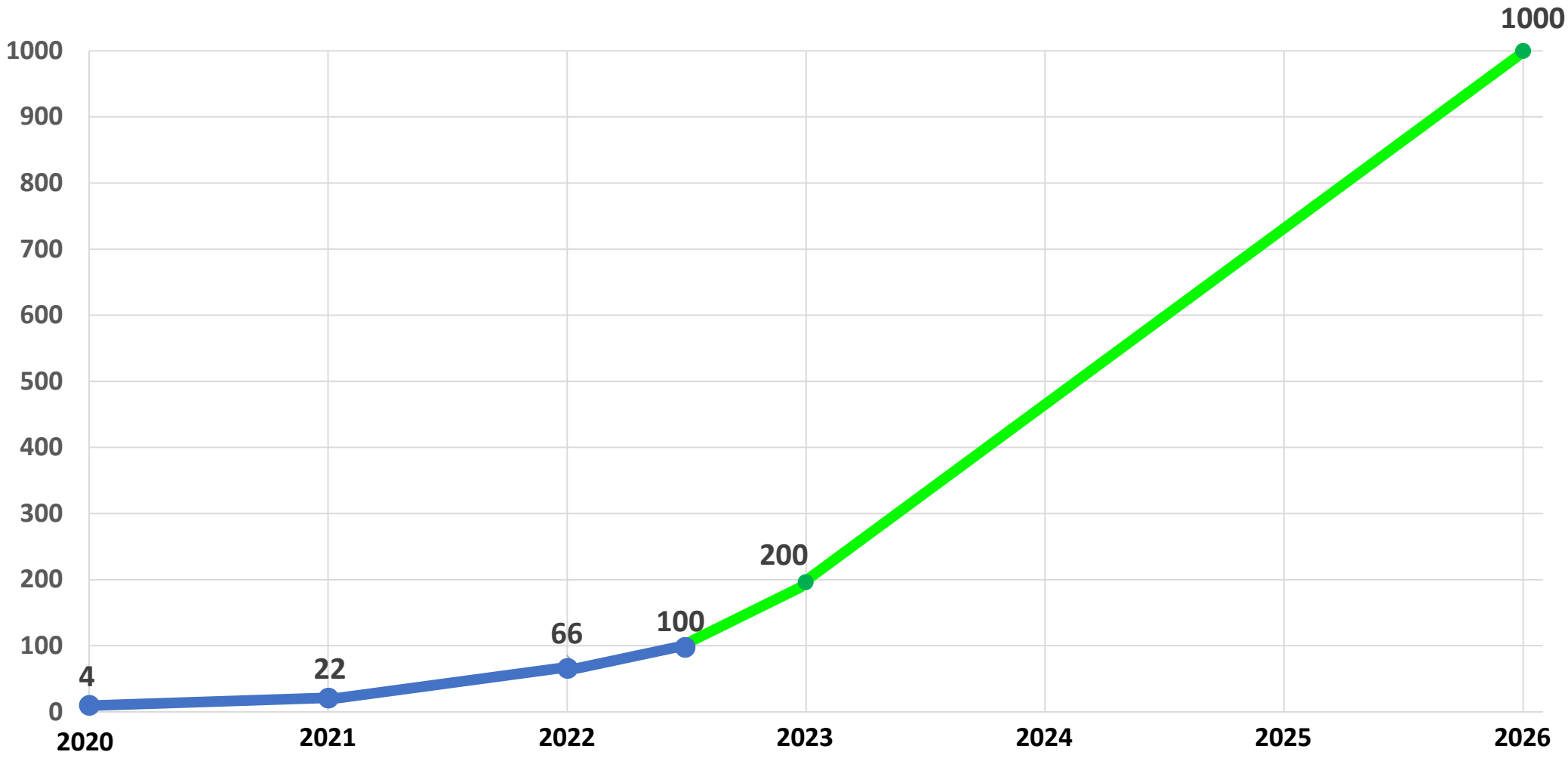
Headcount evolution 2020-2025



PARTNERSHIPS

GRAPHCORE

Atos

intel

More Coming Soon!

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Roadmap toward sovereignty

SIPEARL CORPORATE VISION AND STRATEGY

HPC Supercomputing

SiPearl entry business: European HPC

2023

Data Center-Central

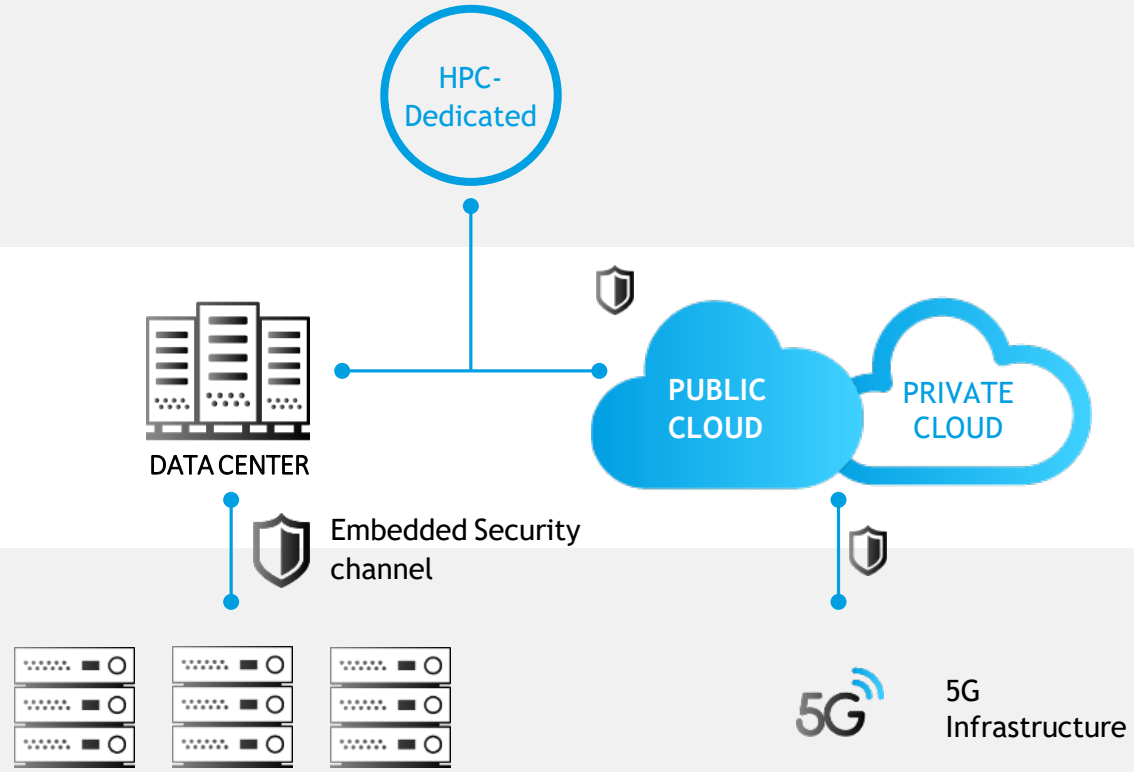
Data centers, private and public cloud

2025

Data Center-Edge

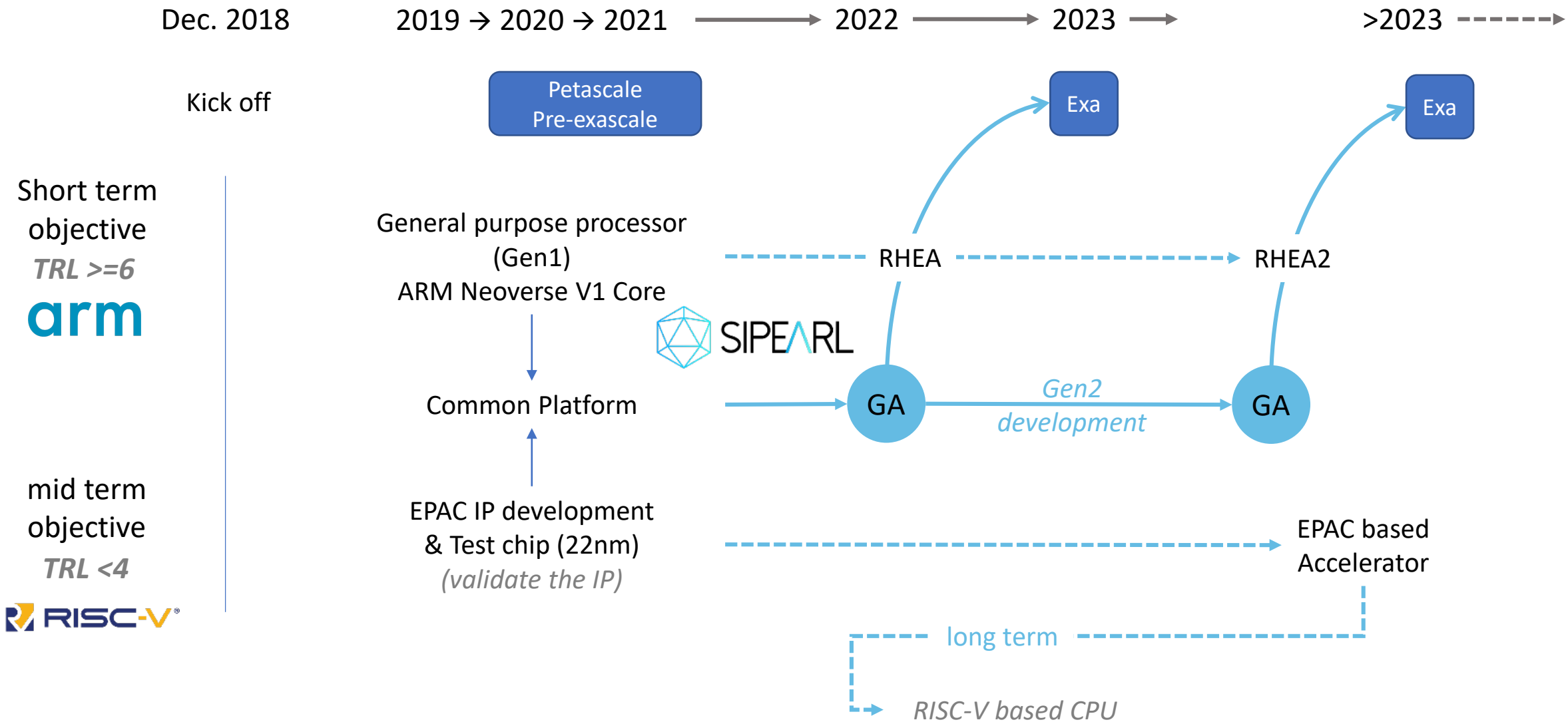
Smaller Data centers, incl around 5G infrastructure

2027+



Our business model is sustainable over time

OVERALL ROADMAP



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EPI COMMON PLATFORM ENABLES EU ECOSYSTEM

- SiPearl chartered is also to develop the European Ecosystem
- SiPearl shares IP and benefits from IP ecosystem
  - Accelerator development (RISC-V based)
    - AI (tensor)
    - Vector processing
    - Stencil processing
    - FPGA
    - …
  - Packaging
  - IP development
- Staged integration: start with socket-to-socket connections and move into package (multi-chiplets) over time

now

Future (10y?)

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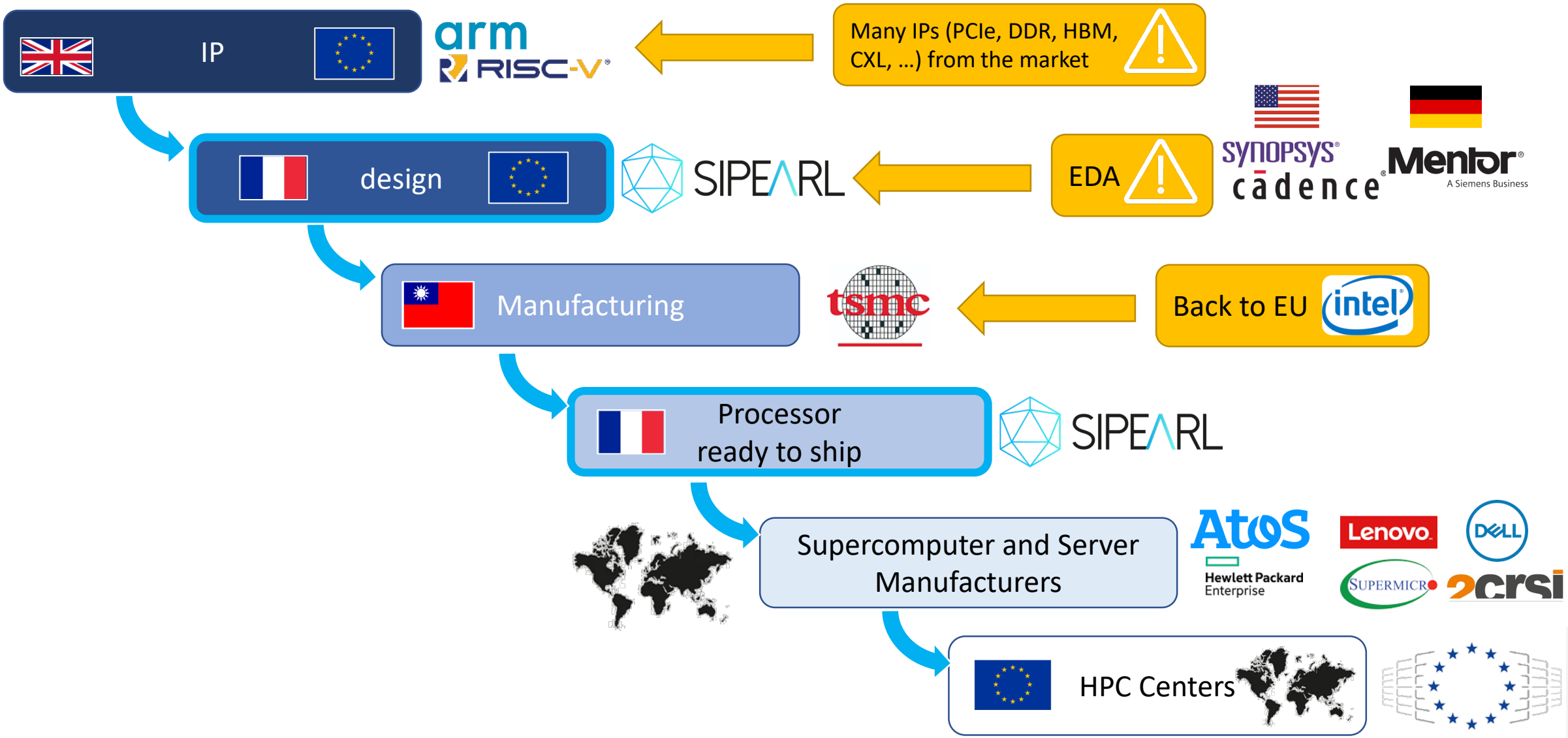
PROCESSOR CORES INSIDE RHEA

	Total: x V1 + 2 M7 Arm, 29 Risc-V, 4x SPUs.	Remarks
Arm Neoverse V1 cores	Arm Neoverse V1	Including spare V1s.
Arm cortex-M7 cores	2x Arm cortex-M7 = 2.	for SCP and MCP subsystems.
Risc-V in PMS	1x Ariane + 1x ZeroRiscy = 2.	
Risc-V in SEG	1x Ariane = 1.	SEG for security element.
Risc-V in STXs of 2x ERACs	2x (1x Ariane + 8x Snitch) = 18.	
Risc-V in VRPs of 2x ERACs	2x (4x VRP core) = 8.	VRP core is a modified Risc-V core.
SPUs in STXs of 2x ERACs	2x (2x SPU cores) = 4.	SPU core is a proprietary core.

- Some additional EU designed IP (power management, clock, cryptography) not counted here
- Not including µC cores used in Synopsys DDR controllers for the PHY training.

Core	Performance for the core.
V1	2x 256 SVE = 16 DP FLOPs/cycle; 2.5GHz@N6
Snitch	1x 64b FPU = 2 DP FLOPs/cycle; >1GHz@N6
SPU	4x 32b FPU = 8 SP FLOPs/cycle; >1GHz@N6

VALUE CHAIN



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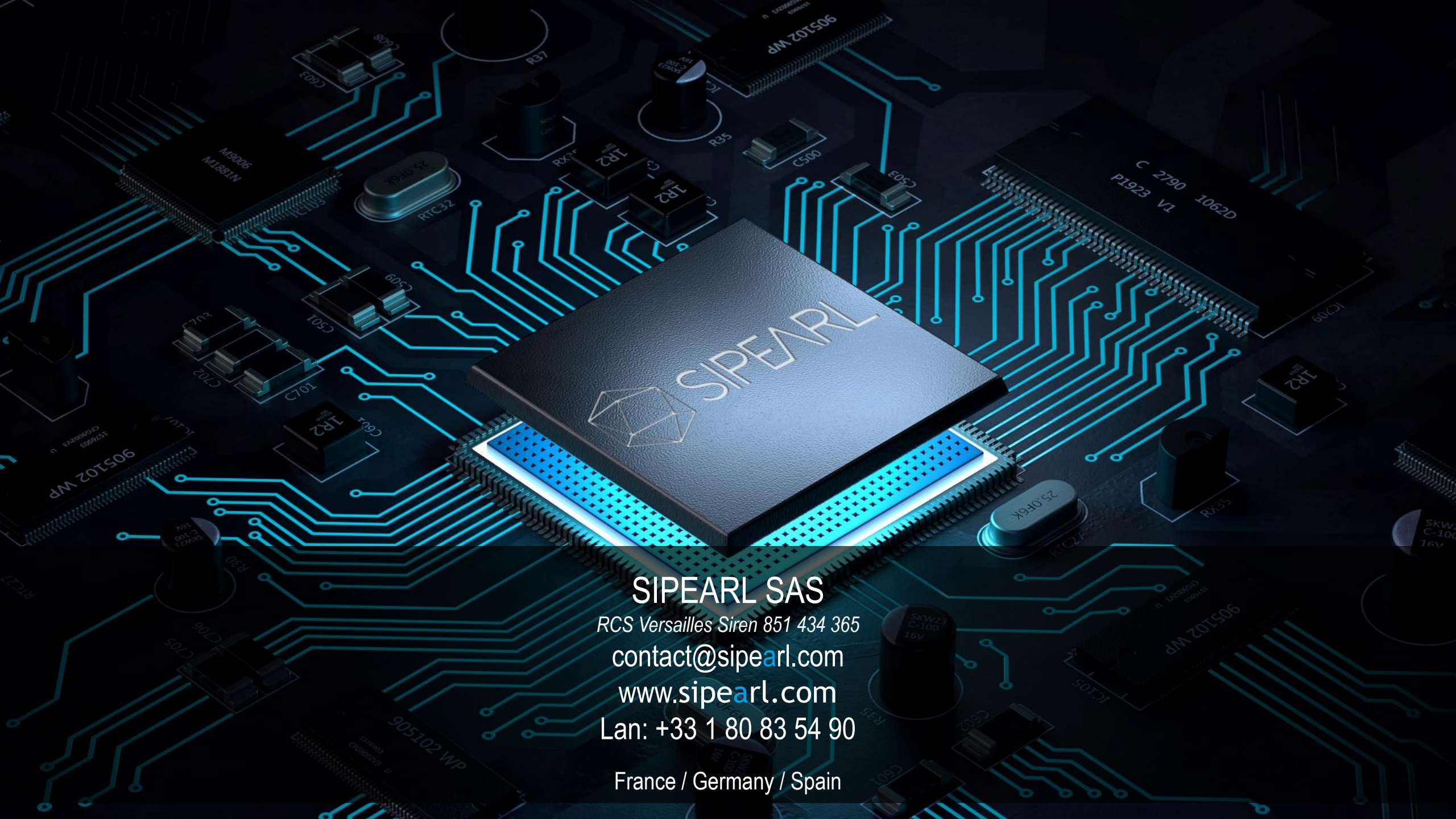

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