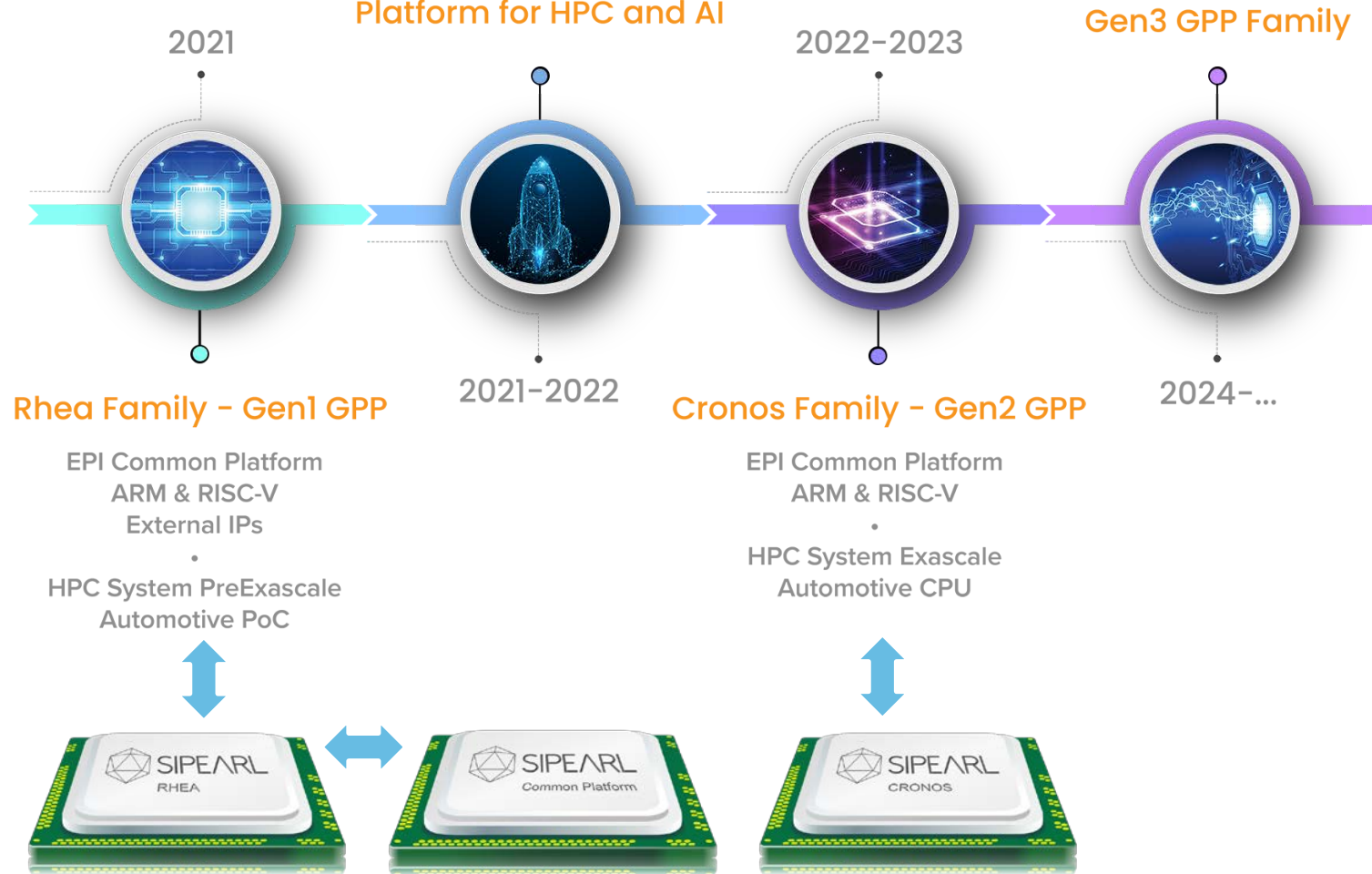


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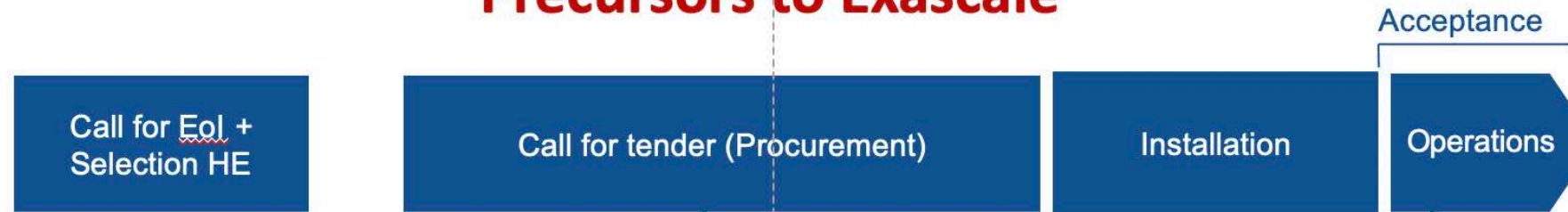


ROADMAP

EPI IP's Launch Pad
&
Pan European Research
Platform for HPC and AI

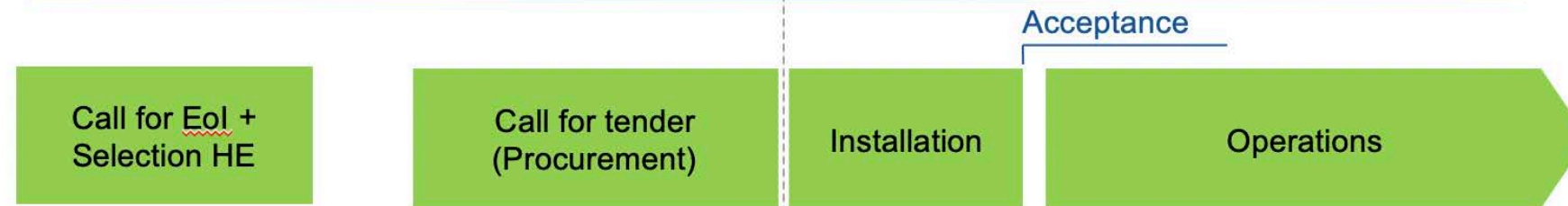


Precursors to Exascale



Access to the JU machines:

- free of charge for publicly funded R&I
- allocation of access time based on calls and peer reviews
- up to 20% of access time for pay-per-use commercial services



2019

2020



Rhea Family - Gen1 GPP

EPI Common Platform
ARM & RISC-V
External IPs

PILOT OBJECTIVES

- Prepare the arrival of EPI technologies
- Test / develop ARM/SVE general purpose processor technologies.
 - Existing ARM based GPP
 - Focus on SW
- Test / develop HPC DP vectorial Accelerators based on RISC-V instruction set
- Exascale applications are workflows → several compute engines
 - Test / develop technologies integrating one well chosen GPP (ARM) + different accelerators (GPU, RISC-V, FPGA, ..)
 - Focus on workflows (usage model) and middleware
 - Focus on seamless / seamless offload

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